

CM6114

Advance Information Single-Channel Transient Voltage Suppressor

Product Description

The CM6114 is an *Application Specific Integrated Passive™* (ASIP™) component in a 2 x 2, 4-bump, 0.4 mm pitch, CSP form factor. This device is designed for:

- Fuse
- Transient Voltage Suppression (TVS)
- Electrostatic Discharge Protection
- Electrical Overstress Protection

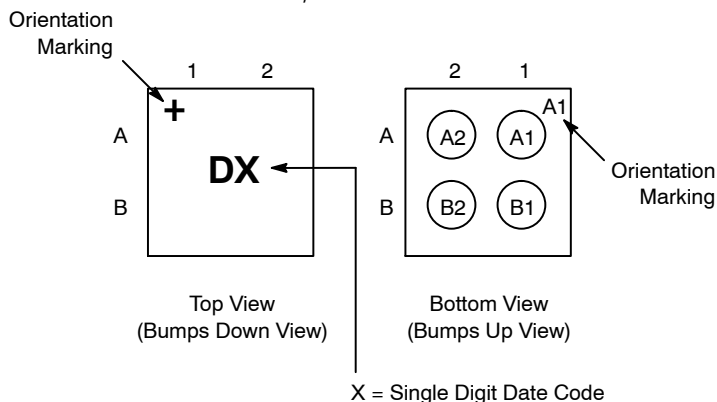
Features

- 4-Bump, 0.8 mm X 0.8 mm Footprint Chip Scale Package (CSP)
- These Devices are Pb-Free and are RoHS Compliant

Table 1. PIN DESCRIPTIONS

4-bump CSP Package	
Pin	Description
A1	Fuse Terminal 1
A2	TVS Channel / Fuse Terminal 2
B1 and B2	Device Ground

PACKAGE / PINOUT DIAGRAMS



4-Bump CSP Package



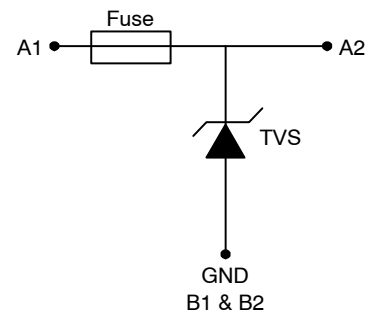
ON Semiconductor®

<http://onsemi.com>



WLCSP4
CASE 567CB

ELECTRICAL SCHEMATIC



MARKING DIAGRAM



D = CM6114
X = Single Digit Date Code

ORDERING INFORMATION

Device	Package	Shipping†
CM6114	WLCSP4 (Pb-Free)	10,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

CM6114

ELECTRICAL SPECIFICATIONS AND CONDITIONS

Table 2. PARAMETERS AND OPERATING CONDITIONS

Parameter	Rating	Units
Storage Temperature Range	-55 to +150	°C
Operating Temperature Range	-30 to +85	°C

Table 3. ABSOLUTE RATINGS

Parameter	Rating	Units
Failing to nonconductive, I^2t – from A1 pin to device ground (Maximum I_{PP} value using 10/1000 μ s pulse). See Notes 1 and 2.	4	A
Failing to nonconductive, I^2t – from A2 pin to device ground (Maximum I_{PP} value using 10/1000 μ s pulse). See Notes 1 and 2.	100	A

1. The device must not burn to open-circuit, when the value is below maximum I_{PP} .
2. This parameter is characterized at 25°C using an ON Semiconductor-specific test board.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R	Resistance A1 – A2	B1 and B2 floating; $T_A = 25^\circ\text{C}$ (Note 2)			50	m Ω
R _{OPEN}	Resistance after open fuse	B1 and B2 floating; $T_A = 25^\circ\text{C}$	1			M Ω
t _{FUSE}	Fusing time	B1 and B2 floating; $I = 5\text{ A}$; $T_A = 25^\circ\text{C}$ (Note 3)			100	ms
t _{LIFE}	Fuse life time	B1 and B2 floating; $I = 2\text{ A}$; $T_A = 25^\circ\text{C}$ (Notes 3 and 4)	4000			Hours
I _{OFF}	Stand-off quiescent current	From A1 pin to B1 and B2 pins; Stand-off voltage $V_{OFF} = 8\text{ V}$; $T_A = 25^\circ\text{C}$			100	nA
V _{BR}	Break down voltage	From A1 pin to B1 and B2 pins; Break down current $I_{BR} = 15\text{ mA}$	10			V
V _{CL}	Clamping voltage during transient	From A1 pin to B1 and B2 pins; Clamping current $I_{CL} = 1\text{ A}$ (Note 5)			13.5	V
V _F	Forward voltage	From A1 pin to B1 and B2 pins; Forward current $I_F = 850\text{ mA}$			1.3	V
C _{L1}	Line capacitance	$V_{BIAS} = 0\text{ V}$		280		pF
C _{L2}		$V_{BIAS} = 5\text{ V}$; $T_A = 25^\circ\text{C}$	108	135		pF
V _{ESD}	ESD protection peak discharge Voltage at A1 pin or A2 to B1 and B2 a) Contact Discharge per IEC 61000-4-2 standard b) Air Discharge per IEC 61000-4-2 standard	$T_A = 25^\circ\text{C}$ (Note 6)				kV
f _C	Minimum attenuation Freq = 80 MHz – 1 GHz Freq = 1 – 4 GHz	$R_{SOURCE} = R_{LOAD} = 50\ \Omega$ $T_A = 25^\circ\text{C}$		12 20		dB

1. All parameters specified for $T_A = -30^\circ\text{C}$ to 85°C unless otherwise noted.
2. This parameter is measured using low current to avoid self-heating.
3. These parameters are characterized using ON Semiconductor-specific test boards.
4. Fuse is considered failed when its resistance is higher than 1 Ω .
5. Transient: 8 x 20 μ s current pulse.
6. Standard IEC 61000-4-2 with $C_{Discharge} = 150\text{ pF}$, $R_{Discharge} = 330\ \Omega$.

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RF CHARACTERISTICS

T_A = 25°C, 50 Ω Environment

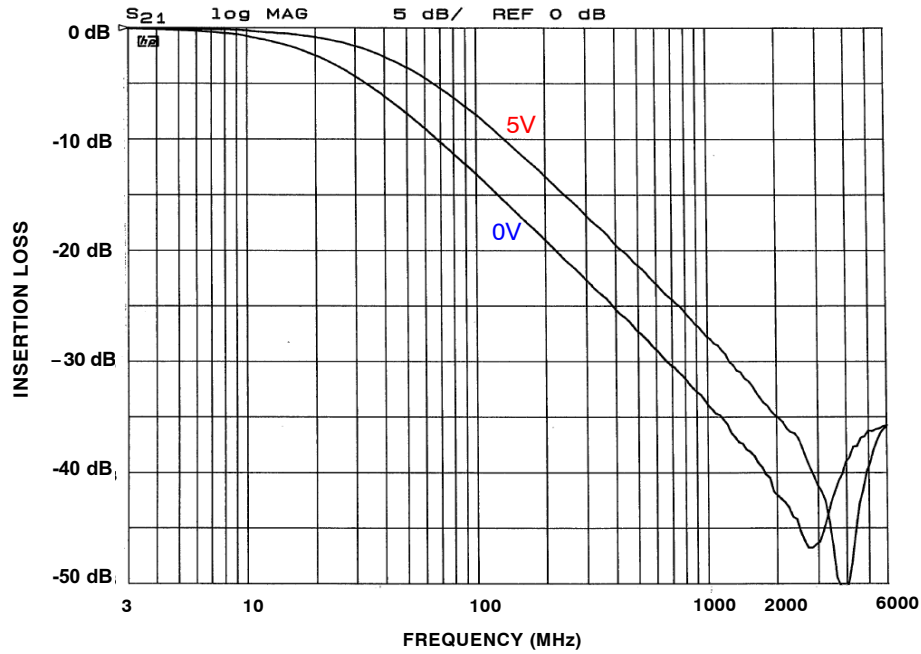


Figure 1. Insertion Loss (0 V and 5 V Bias)

MECHANICAL SPECIFICATION

Table 5. VERTICAL STRUCTURE DIMENSIONS (nominal)

Ref.	Parameter	Material	Dimension
a	Die Thickness	Silicon	389 μm
h	Dielectric Layer 1	Polyimide	7 μm
j	Dielectric Layer 2	Polyimide	10 μm
d	UBM-(Ti/Cu)	Plated Cu	6.5 μm
		Sputtered Cu	0.4 μm
		Sputtered Ti	0.1 μm
e	UBM Wetting Area Diameter		240 μm
b	Bump Standoff		194 μm
f	Solder Bump Diameter after Bump Reflow		270 μm
c	Metal Pad Height	AlSiCu	1.5 μm
g	Metal Pad Diameter		60 μm
D2			0.406 mm
D1	Total Thickness		0.600 mm

Vertical Structure Specification*

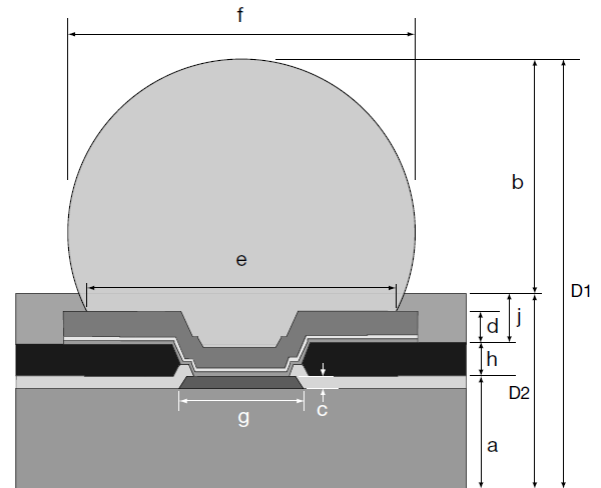


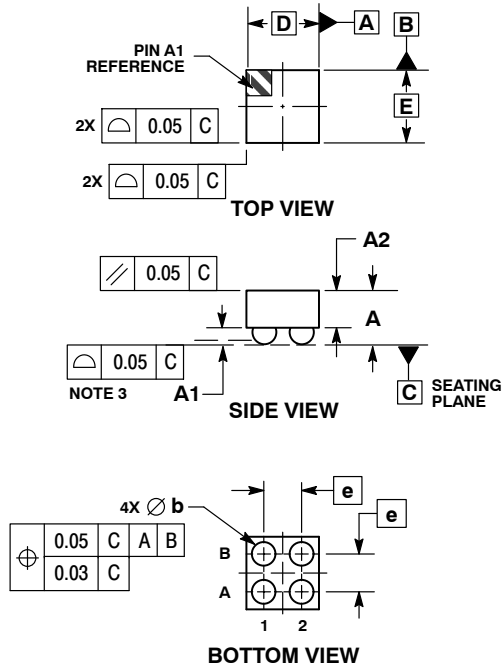
Figure 2. Sectional View

* Daisy Chain CM6040

CM6114

PACKAGE DIMENSIONS

WLCSP4, 0.8x0.8
CASE 567CB-01
ISSUE O

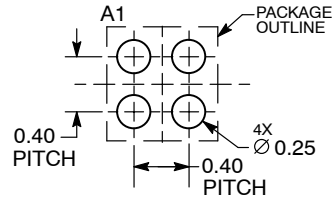


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.57	0.63
A1	0.17	0.24
A2	0.41	REF
b	0.24	0.29
D	0.80	BSC
E	0.80	BSC
e	0.40	BSC

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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